

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant :	David Qiang Meng	Art Unit :	2187
Serial No. :	10/750,423	Examiner :	Jared Ian Rutz
Filed :	December 30, 2003	Conf. No. :	4620
Title :	PARTITIONING MEMORY		

**Mail Stop Appeal Brief - Patents**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

SUPPLEMENTAL REPLY BRIEF

Pursuant to 37 C.F.R. § 41.41, Applicant responds to the Examiner's Supplemental Answer as follows.

In the Supplemental Examiner's Answer, the Examiner states that "[t]he Reply Brief raises new issues not presented in the Appeal Brief submitted 6/18/2007." Appellant respectfully disagrees and contends that no new issues were raised in the previous Reply Brief. The examiner does not however point out any instances of new argument but merely appears to use this as an opportunity to buttress arguments raised in the prior Examiner's Answer.

The Examiner then states:

**Insofar as it is clear, Appellant would have the Board believe that the mere partitioning of a CAM is sufficient to provide "a first group of memory entries being 11 accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel" as recited in claim 1. Assuming arguendo [sic] that this were true, the Examiner respectfully points out that the invention recited in claims 21-26 would be anticipated by a prior art network device utilizing a prior art CAM as taught by Handy, as they would only differ from the claimed Invention as to the arrangement of non-functional descriptive material, IP and MAC addresses.<sup>1</sup>**

The Examiner goes on to state:

**However, as is evidenced by Appellant's submitted "Content-addressable memory" article, this is not the case...[T]he second paragraph on page 1 of "Content-addressable memory"...clearly shows that in a conventional CAM, the entire memory is searched to locate the requested data word.**

---

<sup>1</sup> Supplemental Examiner's Answer, Mail Date 2/1/2008, Page 2

**This is also supported by pages 14-15 of the Handy reference. With respect to the Handy reference, specifically figure 1.7, consider an implementation of a CAM having 10 registers and the comparator associated with each register. It would be within the ability of one of ordinary skill in the art to place one type of data in entries 1-5 and a second type of data in entries 6-10. However, when a user supplies a data word, identified as the compare address in figure 1.7 of Handy, that data would be compared to each data word stored in registers 1-10, and accordingly would not provide a first group of memory entries selectable independent of a second group of memory entries as required by independent claim 1. The Specification of the instant Application provides no guidance on how the disclosed invention allows a first group of entries that are accessible in parallel to be selectable independent of a second group of entries that are accessible in parallel.<sup>2</sup>**

Appellant respectfully disagrees with the Examiner and notes that, as repeatedly discussed in previous responses, the Specification of the instant Application provides guidance in “partitioning a memory device to produce a first group of memory entries [to be]... accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel”, as recited in claim 1<sup>3,4</sup>. These partitions are a **matter of association by a CAM manager** of, e.g., IP address ranges to specific entries (e.g., MAC address 0) stored in CAM entry 0, the CAM entry identifies a location in a local memory that stores data (e.g., an Internet Protocol (IP) address).<sup>5</sup> The Examiner, in laying out the argument *supra* with respect to Handy<sup>6</sup>, ignores Appellant’s teachings of the association by the CAM manager. Without these teachings as guidance, the Examiner mistakenly infers that “[some] data would be compared to each data word stored in [the] registers..., and accordingly would not provide a first group of memory entries selectable independent of a second group of memory entries.”

Appellant also disagrees with the Examiner’s contention that “the invention recited in claims 21-26 would be anticipated by a prior art network device utilizing a prior art CAM as taught by Handy, as they would only differ from the claimed Invention as to the arrangement of non-functional descriptive material, IP and MAC addresses.” Nowhere does Handy describe or suggest, let alone teach, the

---

<sup>2</sup> *Id.*, Pages 2-3.

<sup>3</sup> Appeal Brief dated May 28, 2007, Page 10.

<sup>4</sup> Reply Brief dated November 14, 2007, Pages 2-3.

<sup>5</sup> Specification, Page 8, Line 19.

<sup>6</sup> As a separate issue, the Examiner uses for this argument a total of 10 registers. The number of registers within the CAM, however, is required to be a power of two, as the number of binary output pins is the base-two logarithm of the number of registers. Therefore, a CAM consisting of 10 registers is not a practical arrangement. This fact, however, is tangential to the Examiner’s argument.

method recited in claim 1, or similarly, the product of claim 9, the system of claim 18, the packet forwarding device of claim 21, or the CAM of claim 24.

The examiner's reasoning is improper. The examiner has not furnished nor given Appellant notice of any prior art rejections under 35 U.S.C. 102 or 103 in view of the Handy reference. In so doing, the examiner improperly reads limitations into Appellant's claims because neither IP nor MAC addresses are recited in any of these claims. Therefore, while the examiner's argument is predicated on improperly ignoring these limitations, arguing that they are non-functional descriptive material, Appellant respectfully points out that they have neither been recited in the claims nor relied on to distinguish over the prior art.

Therefore, while Appellant contends that Handy neither describes nor suggests the features of these claims, the examiner's reasoning is completely erroneous because this issue is not before the Board. The issue before the Board is whether the claimed subject matter is enabled. The examiner has not furnished any prior art rejections for Appellant to address or for the Board to consider.

The Examiner further states:

**In the second paragraph beginning on page 8, Appellant argues: "a CAM is a memory device and that it is a specialized memory that is implemented by RAM." The Examiner respectfully notes that the Specification of the instant Application does not state that the CAM may be implemented in RAM. Furthermore, Appellant's submitted "Content-addressable memory" article shows that such an embodiment would not satisfy the recited limitation "a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel...The Examiner respectfully submits that if, arguendo [sic], the Specification of the instant Application had disclosed emulating a CAM using RAM, it would not be sufficient to teach the limitation "a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel. As CAM emulated with a RAM requires traversing a tree or generating a hash function to look up entries, it clearly does not teach that a group of entries are accessible in parallel."<sup>7</sup>**

---

<sup>7</sup> Supplemental Examiner's Answer, Mail Date 2/1/2008, Pages 3-4.

Appellant notes that it is well known to those skilled in the art that a CAM is a memory device that is implemented by RAM. Appellant's statement that **"a CAM is a memory device and that it is a specialized memory that is implemented by RAM."** has not been shown by the examiner to be incorrect, and has been amply supported by Appellant. The Examiner subsequent statement that: **"... the Specification of the instant Application does not state that the CAM may be implemented in RAM."** is again irrelevant because it is well established that a patent need not teach, and preferably omits, what is well known in the art.<sup>8</sup>

Appellant again respectfully disagrees that the Specification of the instant Application is not sufficient to teach the limitation **"a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel"**, a contention repeatedly shown in this and the previous Reply Briefs and previous responses to the Office Actions to be false.

The Examiner further states:

**With respect to Appellant's submitted "Partition (database)" article, the Examiner respectfully submits that it is not germane to the claimed invention. The submitted article is clearly directed to partitioning the tables of a database, and has nothing to do with partitioning a memory device to obtain "a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel."**<sup>9</sup>

Appellant submitted the article on "partitioning" to show that partitioning is a well-known concept. Of course, had Appellant submitted an article that showed: **"with partitioning a memory device to obtain "a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel."**, that would mitigate against a finding of patentability over the prior art.

---

<sup>8</sup> See *In re Buchner*, 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991); *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed. Cir. 1986), cert. denied, 480 U.S. 947 (1987); and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1463, 221 USPQ 481, 489 (Fed. Cir. 1984).

<sup>9</sup> *Id.*, Page 5.

The Examiner goes on to state:

**With respect to Appellant's submitted "Content-Addressable Memory v5.1", it is unclear what Appellant considers relevant from this document. There does not seem to be any discussion of partitioning a memory device. With respect to this document's teaching regarding ternary mode, the Examiner respectfully notes that a CAM operating in ternary mode does not prevent any entry or subentry from being accessed, it merely makes the result of the comparison of selected bits of an entry not considered when determining if an entry matches the input data.<sup>10</sup>**

Appellant noted that the general concept of "partitioning" of memory is well-known to those skilled in the art, as evidenced by the prior submissions. Appellant has claimed a specific type of partitioning and has enabled those of ordinary skill in the art to provide the claimed partitioning.

Therefore, for these reasons, and the reasons stated in the Appeal Brief and the Reply Brief, Appellant submits that the final rejection should be reversed.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: March 17, 2008

/Denis G. Maloney/  
Denis G. Maloney  
Reg. No. 29,670

Fish & Richardson P.C.  
225 Franklin Street  
Boston, MA 02110  
Telephone: (617) 542-5070  
Facsimile: (617) 542-8906

21859783.doc

---

<sup>10</sup> Id.